An Electrolytic Capacitor-Free Half Bridge Class-D Audio Amplifier System Without Bus-Voltage Pumping

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***Abstract*—Conventional half bridge class-D audio amplifier (HB-CDAA) systems typically suffer from serious bus-voltage pumping. Such a bus-voltage pumping increases the device stress and deteriorates the total harmonic distortion and noise (THD+N) of HB-CDAA. To reduce the bus-voltage pumping of HB-CDAA system, large electrolytic capacitors are usually required at the input of downstream HB-CDAA, which seriously affects the power density of HB-CDAA system. In this article, an electrolytic capacitor-free HB-CDAA system without bus-voltage pumping is proposed, which consists of a front-end bipolar-symmetric-outputs (BSO) bidirectional dc–dc converter and a downstream HB-CDAA. By providing a bidirectional current flowing path in the front-end dc–dc converter, the bus-voltage pumping of the HB-CDAA system is eliminated without using large electrolytic capacitors. Zero voltage switching (ZVS) of all switches in the front-end BSO dc–dc converter can be achieved over the full audio load range. Compared with the HB-CDAA system with a unidirectional front-end dc–dc converter, the proposed audio amplifier system benefits from high power density, low-output voltage THD+N, and voltage stress of switches. The bus-voltage pumping problem is identified, the operation of the proposed HB-CDAA system is analyzed, and the design parameters of the converter are derived to ensure ZVS of all switches. Experimental results with a 40-W prototype of the proposed audio amplifier system are presented to verify the design.**

***Index Terms*—Bus-voltage pumping, class-D audio amplifier, dc–dc converter, soft switching.**

I. Introduction

In RECENT years, class-D power amplifiers have attracted more and more attention in audio amplifier applications due to its low total harmonic distortion and noise (THD+N), small volume, high power density, and high conversion efficiency [1]. In some portable audio amplifier, home audio amplifier, professional audio amplifier, and car audio amplifier applications, many audio speakers are usually used to provide high fidelity and stereophonic sound. Each speaker requires one audio amplifier [2], [3]. There are two types of class-D audio amplifiers, full-bridge class-D audio amplifier (FB-CDAA) and half bridge class-D audio amplifier (HB-CDAA). Compared with FB-CDAA, HB-CDAA is more popular in multispeaker audio amplifier system, because the number of switches and driver ICs of HB-CDAA is half of that of FB-CDAA [4], [5].

Usually, switching power supplies are used as the front-end power supply to provide a stable bus voltage to the audio amplifier system [1]. A high-quality front-end power supply is required for low THD+N of the audio amplifier [6]–[9]. Generally, in audio amplifier systems, an isolated front-end dc–dc converter is used in grid powered applications. Nonisolated dc–dc converters can be used in the battery-powered applications or as the second stage dc–dc converter connected to a front-end isolated PFC converter. In a nonisolated dc–dc converter, a boost converter or buck converter can be used as front-end converter for HB-CDAA system. However, the HB-CDAA system with unipolar front-end converter suffers from drawbacks such as requirement of common-mode reference generator, high-power supply rejection ratio (PSRR), and large dc blocking capacitor [10], [11]. Furthermore, for HB-CDAA system with unipolar front-end converter, large dc blocking electrolytic capacitor is required to prevent speaker damage from a large dc voltage. This is not desired for compact size design of audio amplifier system [11].

Compared with HB-CDAA system with front-end unipolar dc–dc converter, HB-CDAA system with front-end symmetric bipolar power supply can remove large dc blocking capacitor, which improves its power density. In [11]–[14], boost and buck–boost converters are used as bipolar front-end dc–dc converter to provide positive and negative output voltage, respectively. In [15], a bipolar dc–dc converter based on conventional three-level-boost is proposed. In [16] and [17], a bipolar output dc–dc converter with two transformer secondaries is proposed for the HB-CDAA system, which achieves ZVS of switches and has no dc magnetizing current for the transformer.

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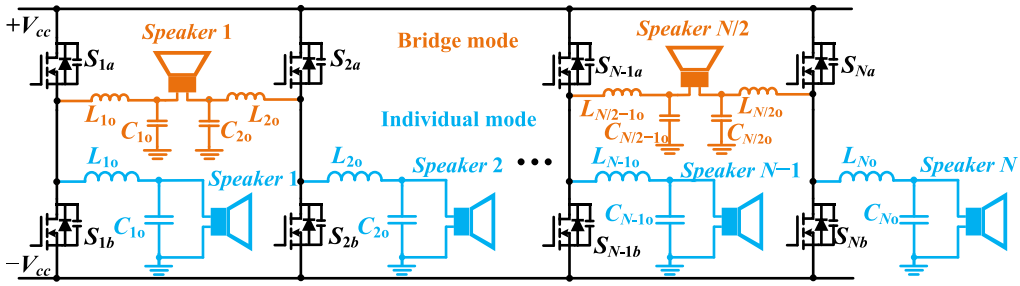


Fig. 1. Circuit diagram of a multichannels CDAA system in [31].

Unidirectional dc–dc converters are usually used as the front-end converter for HB-CDAA system in [11]–[18], which has severe bus-voltage pumping on power supply of class-D amplifier [19]. When output audio frequency is lower than 200 Hz, the pumping voltage can become several times greater than the bus voltage, which increases device voltage stress. In addition, high power supply ripple has negative effects on output THD+N of audio amplifier [20]. Thus, large electrolytic capacitors are generally used to reduce the bus-voltage pumping in HB-CDAA systems.

In [21]–[24], several control strategies have been proposed to achieve high PSRR to improve THD+N of audio amplifiers. However, if bus-voltage pumping is severe or the bipolar power supply of HB-CDAA is asymmetric, higher PSRR is required to maintain the same THD+N of an audio amplifier system with a stable bipolar power supply. This increases complexity of the audio amplifier controller. In order to reduce the complexity of the controller, a HB-CDAA system with front-end symmetric bipolar outputs *LLC* dc-transformer (DCX) converter is presented in [25]. However, unidirectional DCX cause severe bus-voltage pumping, which reduces the system efficiency and increases the voltage stress of the class-D audio amplifier [25]. A bidirectional DCX is presented in [26] to eliminate the bus-voltage pumping in HB-CDAA system. As a front-end DCX cannot adjust output voltage, the bus-voltage pumping is transferred to the input power supply, large electrolytic capacitors are still required at the input power supply to provide a relatively stable bus voltage for downstream HB-CDAA [26].

For the high-frequency-link audio amplifier systems proposed in [27]–[30], a bidirectional current flowing path is provided to reduce bus-voltage pumping. However, multi speakers are usually required to generate high fidelity and stereophonic sound in audio amplifier system. For example, ten speakers are required in a Dolby Atmos 7. 1. 6 system [3]. If ten high-frequency-link audio amplifiers are used, more than 80 switches are required in total, which has very high cost.

Generally, in a CDAA system, both individual mode and bridge mode are supported in multichannels CDAA products [5], [31], [32]. Individual mode operates with HB-CDAA, which is suitable for light load. Bridge mode operates with FB-CDAA, which consists of two individual HB-CDAA and are suitable for heavy load. As shown in Fig. 1, *N* HB-CDAAs can drive *N* speakers with individual mode as shown in blue speakers, or *N* HB-CDAAs can drive *N*/2 speakers with bridge mode as shown in yellow speakers. For example, a 16 channels CDAA system only can run a Dolby Atmos 7.1 system with FB mode, but with individual mode, an 8 channels CDAA system is enough for a Dolby Atmos 7.1 system [31], [32].

As most of CDAA products support HB-CDAA individual mode, a front-end symmetric bipolar outputs dc–dc converter with no bus-voltage pumping and without large electrolytic capacitors is a prospective solution in establishing the CDAA system.

In this article, an electrolytic capacitor-free HB-CDAA system with bus-voltage pumping elimination is proposed. In the proposed audio amplifier system, ZVS of switches of front-end converter can be achieved over the entire load current range. The front-end converter has step-up or down bipolar symmetric voltage gains. Therefore, high efficiency, high power density, and low output voltage THD+N are achieved.

The rest of this article is organized as follows. Section II analyses the bus-voltage pumping problem of conventional HB-CDAA systems. Operation principle of the proposed HB-CDAA system is presented in Section III. Steady state analysis, including voltage gain, voltage, and current stress and soft switching condition, are given in Section IV. Section V presents the controller design. Experimental results and conclusion are given in Sections VI and VII, respectively.

II. Analysis of Bus-Voltage Pumping in the Conventional HB-CDAA

A. Bus-Voltage Pumping in HB-CDAA

Fig. 2 shows an HB-CDAA system with a front-end unidirectional bipolar output dc–dc converter. If the ripple current is neglected, the load current $i_{speaker}$ flowing through the speaker is equal to current i_{Lo}, and i_{Lo} is equal to $i_{Sa}-i_{Sb}$. The HB-CDAA system can therefore be considered as a load of the front-end bipolar output dc–dc converter, that are two current sources $i_{load,p}$ and $i_{load,n}$ shown in Fig. 3(a) and (b).

From Fig. 3 it can be known that when $i_{load,p} < 0$, current $i_{load,p}$ is blocked by diodes D_1, and when $i_{load,n} < 0$, current $i_{load,n}$ is blocked by diodes D_2. Thus, the output capacitors C_{pos} and C_{neg} of the front-end converter are charged and produce bus-voltage pumping.

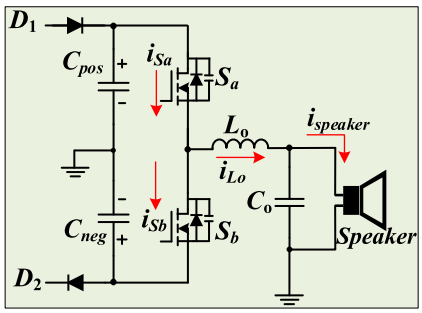


Fig. 2. HB-CDAA system with a front-end unidirectional bipolar output dc–dc converter.

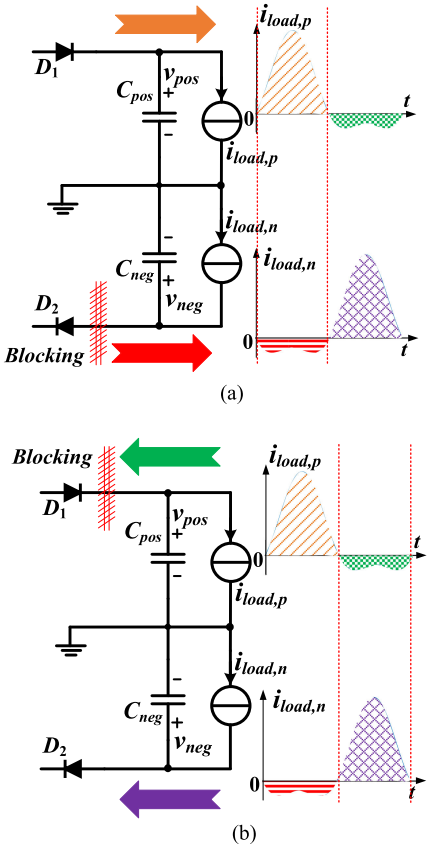


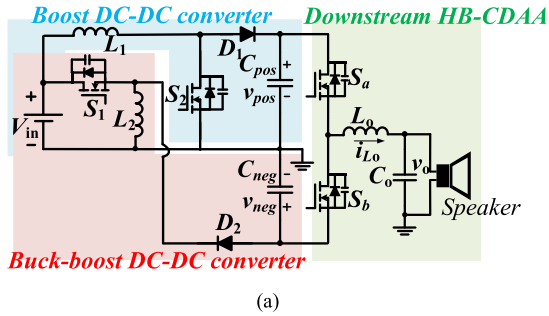
Fig. 3. Bus-voltage pumping of a conventional HB-CDAA system. (a) Current flowing paths in conventional HB-CDAA system when current i_{Lo} is positive. (b) Current flowing paths in the conventional HB-CDAA system when current i_{Lo} is negative.

From [25], $i_{load,p}$ and $i_{load,n}$ are obtained as

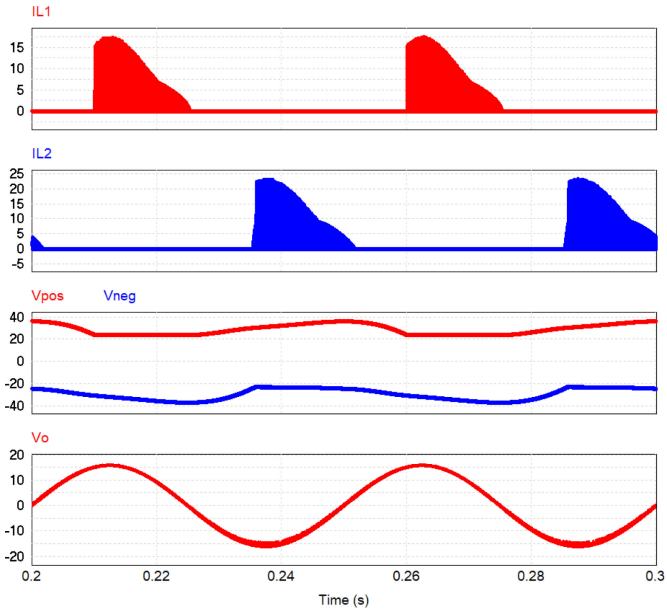
$$\begin{cases} i_{load,p}(t) = [\frac{1}{2} + \frac{1}{2}m\sin(\omega t)]\frac{mV_{bus}\sin(\omega t+\varphi)}{|Z_{speaker}|} \\ i_{load,n}(t) = -[\frac{1}{2} - \frac{1}{2}m\sin(\omega t)]\frac{mV_{bus}\sin(\omega t+\varphi)}{|Z_{speaker}|}. \end{cases} \quad (1)$$

Thus, pumping voltages across bus capacitors C_{pos} and C_{neg} are

$$\Delta v_{pos} = \frac{\int_{\frac{\pi-\varphi}{\omega}}^{\frac{2\pi-\varphi}{\omega}} -i_{load,p}(t)dt}{C_{pos}} = \frac{mV_{pos}(4 - m\pi\cos\varphi)}{8\pi f_o\,|Z_{speaker}|\,C_{pos}} \quad (2)$$



(a)



(b)

Fig. 4. HB-CDAA system with conventional unidirectional bipolar front-end dc–dc converter and its key waveforms. (a) HB-CDAA system with conventional unidirectional bipolar front-end dc–dc converter in [12]–[14]. (b) Key simulated waveforms in PSIM.

$$\Delta v_{neg} = \frac{\int_{\frac{-\varphi}{\omega}}^{\frac{\pi-\varphi}{\omega}} -i_{load,n}(t)dt}{C_{neg}} = \frac{|-mV_{neg}(4 - m\pi\cos\varphi)|}{8\pi f_o\,|Z_{speaker}|\,C_{neg}} \quad (3)$$

where m is the modulation index of the class-D audio amplifier, V_{bus} is the power supply voltage of the class-D audio amplifier, which equals to the magnitude of V_{pos} and V_{neg}, ω is the angular frequency of the output voltage of the audio amplifier, φ is the phase difference between the output current and output voltage of the audio amplifier, and $Z_{speaker}$ is the impedance of the speaker.

If bus-voltage pumping voltage $\Delta v_{pos} = \Delta v_{neg} = 24$ V is expected, when $m = 0.74$, $V_{pos} = 24$ V, $|Z_{speaker}| = 4\ \Omega$, $\varphi = \pi/6$, and $f_o = 20$ Hz, capacitors with capacitance $C_{pos} = C_{neg} = 736\ \mu$F/48 V are required. Accordingly, the power density of the audio amplifier system is reduced with such a large electrolytic capacitor.

Fig. 4(a) shows a conventional HB-CDAA system with a typical unidirectional bipolar front-end dc–dc converter in [12]–[14]. A boost converter is used to provide positive bus voltage

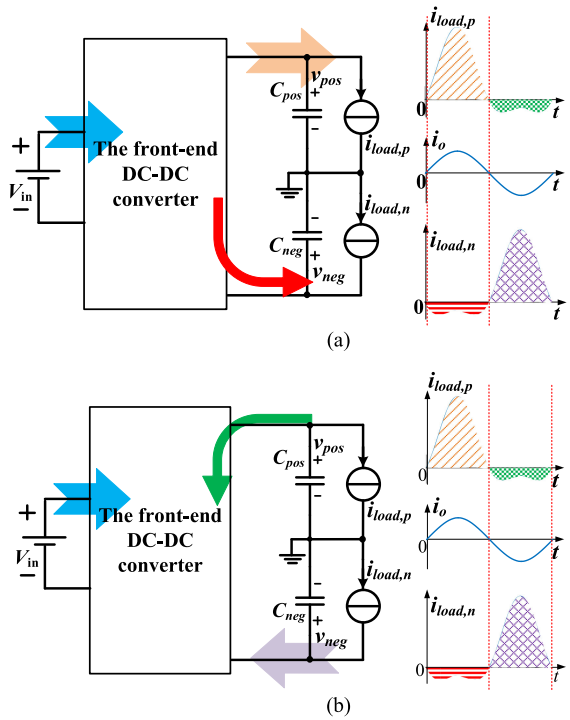


Fig. 5. Diagram of current flowing paths in a HB-CDAA system with bidirectional bipolar front-end dc–dc converter. (a) When load current $i_o > 0$. (b) When load current $i_o < 0$.

for downstream HB-CDAA, and a buck–boost converter is used to provide negative bus voltage.

As shown in Fig. 4(b), it still has severe bus-voltage pumping although 1200-μF bus capacitors are used. When bus-voltage pumping is occurred and positive bus voltage is higher than the designed positive bus voltage, the boost converter would reduce its duty cycle to approximately zero and stop transferring energy from input to output. Similarly, the buck–boost converter would also reduce its duty cycle to approximately zero and stop transferring energy from input to output when negative bus voltage is lower than designed negative bus voltage. As unidirectional bipolar front-end dc–dc converter can only transfer power from input to load when there is no bus-voltage pumping, peak values of inductor currents i_{L1} and i_{L2} become very large, which increases current stress and reduces efficiency of the audio amplifier system.

B. Elimination of Bus-Voltage Pumping of HB-CDAA

Compared with conventional HB-CDAA as shown in Fig. 4(a), a bidirectional current flowing path is provided in a HB-CDAA system with a bidirectional bipolar front-end dc–dc converter. According to (1), Fig. 5(a) and (b) shows current flowing paths when load current $i_o > 0$ and $i_o < 0$, respectively. When $i_{load,n} < 0$, the bidirectional front-end dc–dc converter would provide a current flowing path for $i_{load,n}$ to keep the negative bus voltage stable. When the current $i_{load,p} < 0$, backward current from $i_{load,p}$ would flows through the bidirectional front-end dc–dc converter to keep positive bus voltage stable. Thus, the bus-voltage pumping is eliminated.

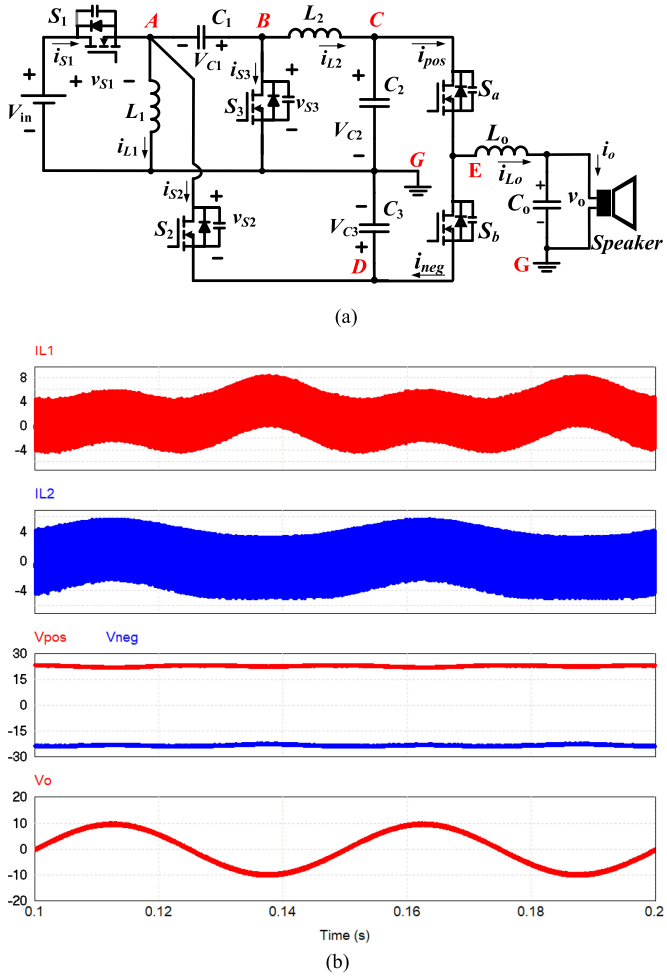


Fig. 6. Proposed HB-CDAA system and its key waveforms. (a) The proposed HB-CDAA system. (b) Key simulated waveforms in PSIM.

Conventional designs utilize large bus capacitor to tackle with bus-voltage pumping [25]. However, the large volume of the electrolytic capacitor would also reduce the power-density of the amplifier system. If the bidirectional current flowing paths are provided in the front-end dc–dc converter, the bus-voltage pumping can be eliminated. A soft-switching bidirectional DCX is presented in [26] to eliminate the bus-voltage pumping; however, this DCX cannot adjust output voltage. This means the bus-voltage pumping is transferred to the input power supply, and large electrolytic capacitors are still required at the input.

In order to overcome the defects faced by conventional solutions, a novel HB-CDAA system is proposed in this article, which benefits from the bus-voltage pumping elimination, electrolytic capacitor-free in the whole HB-CDAA system, and soft-switching in the front-end dc–dc converter. The detailed description and analysis are described in the following.

III. Operation of the Proposed HB-CDAA System

Fig. 6(a) shows the proposed HB-CDAA system, which consists of bidirectional front-end dc–dc converter and a downstream HB-CDAA. In Fig. 6(a), i_{pos} and i_{neg} represent the simultaneous currents flowing through switches S_a and S_b,

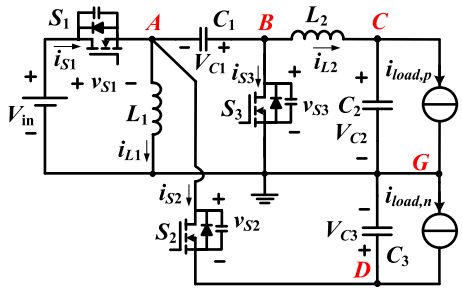


Fig. 7. Equivalent circuit of the proposed HB-CDAA system when downstream class-D is considered as current sources.

respectively. Fig. 6(b) shows that there is no bus-voltage pumping when 47-μF bus capacitors C_2 and C_3 are used. As the front-end dc–dc converter works well all time, currents i_{L1} and i_{L2} are smaller than their counterparts shown in Fig. 4(b), which decreases current stress and improves efficiency.

Fig. 7 shows the equivalent circuit of the proposed HB-CDAA system when a downstream class-D is considered as current sources. In Fig. 7, $i_{load,p}$ and $i_{load,n}$ represent the equivalent load currents at the positive and negative outputs of the proposed front-end dc–dc converter, respectively, when the downstream HB-CDAA is considered as current sources. To simplify the analysis of the proposed HB-CDAA system, the following assumptions are made and small-ripple approximation can be assumed [33].

1) All switches and corresponding body diodes are considered as ideal devices with identical output capacitance ($C_{oss,s1} = C_{oss,s2} = C_{oss,s3} = C_{oss}$).
2) Capacitors $C_1 = C_2 = C_3$ and are large enough that the voltage ripple across them can be neglected.

As the average current i_{L2} is equal to load current $i_{load,p}$, when $i_{load,p} > 0$ and $i_{load,p} < 0$, the operation modes of the proposed HB-CDAA system are different.

Fig. 8(a) and (b) shows key waveforms of the proposed HB-CDAA system when $i_{load,p} > 0$ and $i_{load,p} < 0$, respectively, where t_d is dead time between the driving signal of switches S_1 and S_2∼S_3. When the dead time t_d is neglected, the driving signals of switches S_1 and S_2∼S_3 are complementary. As the operation modes of the proposed HB-CDAA system are similar when $i_{load,p} > 0$ and $i_{load,p} < 0$, only the operation modes when $i_{load,p} > 0$ are analyzed.

In a steady state with $i_{load,p} > 0$, the proposed HB-CDAA system has four operation modes, as shown in Fig. 9.

Mode 1 [t_0–t_1]: Mode 1 is dead time mode. In this mode, switch S_1 is turned OFF and the body diodes of switches S_2 and S_3 are turned ON to provide flowing path for freewheeling currents i_{L2} and i_{L1}.

As mode 1 is very short, i_{L1} and i_{L2} are positive and can be regarded as constant. The output capacitors of switches S_2 and S_3 are discharged, and the output capacitors of switch S_1 are charged. When the output capacitors of switches S_2 and S_3 are discharged completely, the body diode of switches S_2 and S_3 are turned ON and the voltages across switches S_2 and S_3 are zero. Mode 1 ends when switches S_2 and S_3 are turned ON at time t_1.

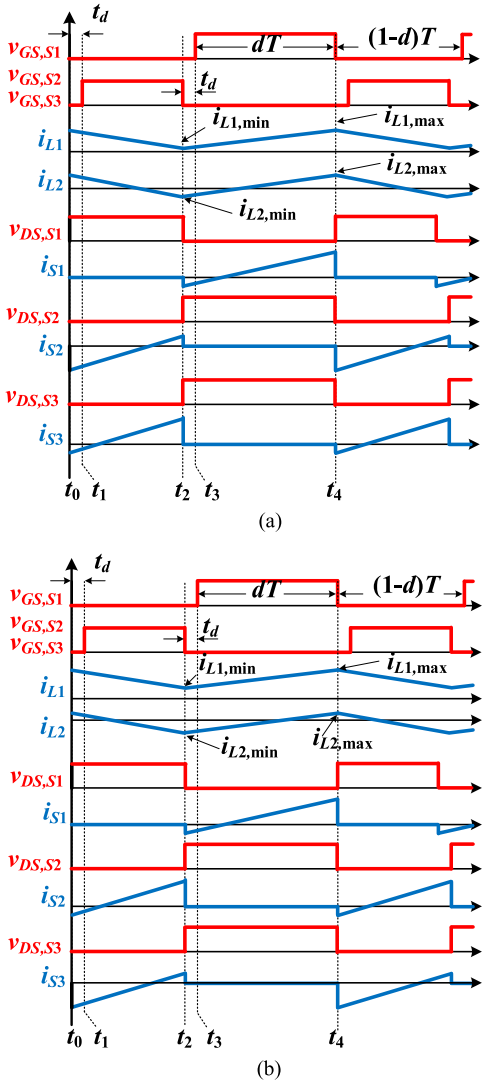


Fig. 8. Key waveforms of the proposed HB-CDAA system. (a) Key waveforms when $i_{load,p} > 0$. (b) Key waveforms when $i_{load,p} < 0$.

To achieve zero voltages across switches S_2 and S_3 by the end of mode 1, the following condition should be met:

$$\int_{t_0}^{t_1} i_{L1}(t)dt + \int_{t_0}^{t_1} i_{L2}(t)dt \approx [i_{L1}(t_1) + i_{L2}(t_1)] \cdot t_d > v_{ds1}(t_0) \cdot C_{oss,\,s_1} + v_{ds2}(t_1) \cdot C_{oss,\,s_2} + v_{ds3}(t_1) \cdot C_{oss,\,s_3}. \quad (4)$$

Mode 2 [t_1–t_2]: At time t_1, as voltages across switches S_2 and S_3 are zero, therefore ZVS turn-ON of switches S_2 and S_3 can be achieved. Currents i_{L1} and i_{L2} decrease and satisfy $(i_{L1}+i_{L2}) < 0$ at time t_2. V_{C1} equals to $-V_{C3}$ because capacitor C_1 is in parallel with capacitor C_3. In this mode, currents i_{L1} and i_{L2} are given as

$$i_{L1}(t) = i_{L1}(t_1) + \frac{V_{C3}}{L_1}t \quad (5)$$

$$i_{L2}(t) = i_{L2}(t_1) - \frac{V_{C2}}{L_2}t. \quad (6)$$

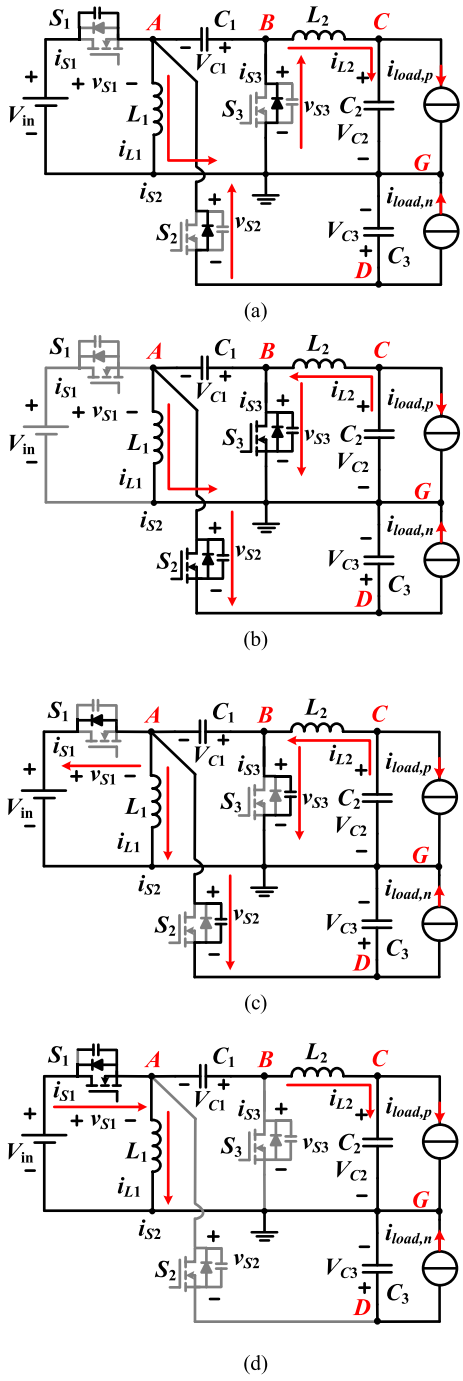


Fig. 9. Operation modes of the proposed HB-CDAA system. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

Voltages V_{C1} and V_{C3} satisfy the following condition:

$$V_{C1} + V_{C3} = 0. \tag{7}$$

Mode 2 ends when switches S_2 and S_3 are turned OFF at time t_2.

Mode 3 [t_2–t_3]: Mode 3 is dead time mode. At time t_2, switches S_2 and S_3 are turned OFF. Because $(i_{L1}+i_{L2}) < 0$, after switches S_1-S_2 are turned OFF, the body diode of switch S_1 is turned ON to provide flowing a path for the freewheeling current $(i_{L1}+i_{L2})$. As mode 3 is very short, i_{L1} and i_{L2} can be regarded as constant. The output capacitor of switch S_1 is discharged, and the output capacitors of switches S_2 and S_3 are charged since $(i_{L1}+i_{L2}) < 0$. When the output capacitor of switch S_1 is completely discharged, the voltage across switch S_1 is zero, and the body diode of switch S_1 is turned ON.

To achieve zero voltage across switch S_1 by the end of mode 3, the following condition should be met:

$$\begin{aligned}\int_{t_2}^{t_3} -[i_{L1}(t) + i_{L2}(t)]dt &\approx -[i_{L1}(t_3) + i_{L2}(t_3)] \cdot t_d \\ &> v_{ds1}(t_2) \cdot C_{oss,\,s_1} + v_{ds2}(t_3) \\ &\cdot C_{oss,\,s_2} + v_{ds3}(t_3) \cdot C_{oss,\,s_3}.\end{aligned} \tag{8}$$

Mode 3 ends when switch S_1 is turned ON at time t_3.

Mode 4 [t_3–t_4]: At time t_3, as the voltage across switch S_1 is zero, ZVS turn-ON of switch S_1 can be achieved. Currents i_{L1} and i_{L2} increase to positive.

In this mode, currents i_{L1} and i_{L2} are given by

$$i_{L1}(t) = i_{L1}(t_3) + \frac{V_{in}}{L_1}t \tag{9}$$

$$i_{L2}(t) = i_{L2}(t_3) + \frac{V_{in} + V_{C1} - V_{C2}}{L_2}t. \tag{10}$$

Mode 4 ends when switch S_1 is turned OFF at time t_4.

IV. Steady-State Characteristics of the Proposed HB-CDAA System

A. Voltage Gain Analysis

If the dead time t_d is neglected, the proposed HB-CDAA system has two operation modes, mode 2 and 4, within each switching period. In a steady state, the volt-second balance of L_1 gives

$$V_{in}dT + V_{C3}(1-d)T = 0. \tag{11}$$

Thus, the voltage across capacitor C_3 is given by

$$V_{C3} = -\frac{d}{1-d}V_{in}. \tag{12}$$

Volt-second balance of L_2 gives

$$(V_{in} + V_{C1} - V_{C2})dT + (-V_{C2})(1-d)T = 0. \tag{13}$$

Substituting (7) into (12) gives

$$V_{C1} = \frac{d}{1-d}V_{in}. \tag{14}$$

Substituting (14) into (13) gives

$$V_{C2} = \frac{d}{1-d}V_{in}. \tag{15}$$

From (12) and (15), the gains of the bipolar symmetric outputs of the front-end BSO dc–dc converter can be obtained as

$$G_n = \frac{V_n}{V_{in}} = \frac{V_{C3}}{V_{in}} = -\frac{d}{1-d} \tag{16}$$

$$G_p = \frac{V_p}{V_{in}} = \frac{V_{C2}}{V_{in}} = \frac{d}{1-d}. \tag{17}$$

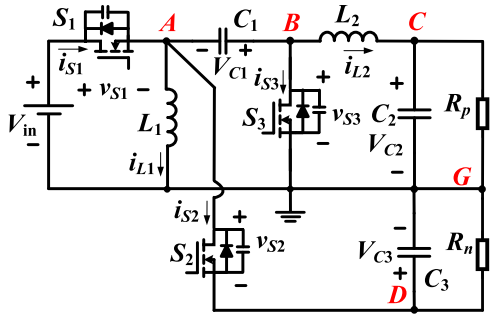


Fig. 10. Equivalent circuit of the proposed HB-CDAA system when the downstream class-D is considered as resistor.

From (16) and (17), it can be known that $G_p = -G_n$, i.e., bipolar-symmetric-outputs with step-up/down are obtained.

B. Voltage and Current Stress Analysis

Fig. 10 shows the equivalent circuit of the proposed HB-CDAA system.

As shown in Fig. 10, as voltages V_{C2} and V_{C3} of the front-end dc–dc converter are constant, the downstream HB-CDAA load can be considered as resistors, as given below

$$R_p = \frac{V_{C2}}{i_{load,p}}, R_n = \frac{V_{C3}}{-i_{load,n}}. \tag{18}$$

The voltage stress of switches S_1, S_2, and S_3 can be obtained from modes 2 and 4 as

$$V_{stress,S_1} = V_{stress,S_2} = V_{in} - V_{C3} = \frac{1}{1-d}V_{in} \tag{19}$$

$$V_{stress,S_3} = V_{in} + V_{C1} = \frac{1}{1-d}V_{in}. \tag{20}$$

According to the ampere-second balance of C_1 and C_2, at node C, average current I_{L2} is

$$I_{L2} = \frac{V_p}{R_p} = \frac{dV_{in}}{(1-d)R_p} \tag{21}$$

and at node D, average current I_{S3} is

$$I_{S3} = I_{L2} = \frac{dV_{in}}{(1-d)R_p}. \tag{22}$$

According to ampere-second balance of C_3, at node D, average current I_{S2} is

$$I_{S2} = \frac{V_n}{R_n} = -\frac{dV_{in}}{(1-d)R_n}. \tag{23}$$

From power conservation, the following equation is derived:

$$V_{in}I_{S1} = \frac{{V_p}^2}{R_p} + \frac{{V_n}^2}{R_n} = \frac{d^2{V_{in}}^2(R_p+R_n)}{(1-d)^2R_pR_n}. \tag{24}$$

From (24), average current I_{S1} is

$$I_{S1} = \frac{d^2V_{in}(R_p+R_n)}{(1-d)^2R_pR_n}. \tag{25}$$

At node A, average current I_{S1} satisfied

$$I_{L1} = I_{S1} - I_{S2}. \tag{26}$$

Substituting (23) and (25) into (26) gives

$$I_{L1} = \frac{d^2V_{in}R_n + dV_{in}R_p}{(1-d)^2R_pR_n}. \tag{27}$$

As can be known from the operation mode analysis, ZVS turn-ON of switch S_1 can be achieved when $(i_{L1}+i_{L2}) < 0$ at time t_3, and ZVS turn-ON of switches S_2 and S_3 can be achieved when $(i_{L1}+i_{L2}) > 0$ at time t_1. In the proposed HB-CDAA system, the current ripples of inductors L_1 and L_2 are

$$\Delta i_{L1} = \frac{V_{in}dT}{2L_1} \tag{28}$$

$$\Delta i_{L2} = \frac{V_{C2}(1-d)T}{2L_2}. \tag{29}$$

Thus, the minimum and maximum currents flowing through inductors L_1 and L_2 are obtained as

$$i_{L_1,\min} = I_{L_1} - \frac{V_{in}}{2L_1}dT = \frac{d^2V_{in}R_n + dV_{in}R_p}{(1-d)^2R_pR_n} - \frac{V_{in}}{2L_1}dT \tag{30}$$

$$i_{L_1,\max} = I_{L_1} + \frac{V_{in}}{2L_1}dT = \frac{d^2V_{in}R_n + dV_{in}R_p}{(1-d)^2R_pR_n} + \frac{V_{in}}{2L_1}dT \tag{31}$$

$$\begin{aligned} i_{L_2,\min} &= I_{L_2} - \frac{V_{in}+V_{C1}-V_{C2}}{2L_2}dT \\ &= \frac{dV_{in}}{(1-d)R_p} - \frac{V_{in}}{2L_2}dT \end{aligned} \tag{32}$$

$$\begin{aligned} i_{L_2,\max} &= I_{L_2} + \frac{V_{in}+V_{C1}-V_{C2}}{2L_2}dT \\ &= \frac{dV_{in}}{(1-d)R_p} + \frac{V_{in}}{2L_2}dT. \end{aligned} \tag{33}$$

C. Soft Switching Analysis

The ZVS condition (8) of switch S_1 is more difficult to satisfy than the ZVS condition (4) of switches S_2 and S_3. Therefore, only ZVS condition (8) of switch S_1 is studied.

Substituting (19), (20), (30), and (32) into (8) gives

$$-\frac{d^2R_n + dR_p}{(1-d)^2R_pR_n} + \frac{dT}{2L_1} - \frac{d}{(1-d)R_p} + \frac{dT}{2L_2} > \frac{3C_{oss}}{(1-d)t_d}. \tag{34}$$

From (34), there is

$$L_e < \frac{dT}{2\left(\frac{3C_{oss}}{(1-d)t_d} + \frac{d}{(1-d)^2R_e}\right)} \tag{35}$$

where $L_e = L_1L_2/(L_1+L_2)$ denotes equivalent inductance of inductor L_1 in parallel with L_2 and $R_e = R_pR_n/(R_p+R_n)$ denotes equivalent resistance of resistor R_p in parallel with R_n.

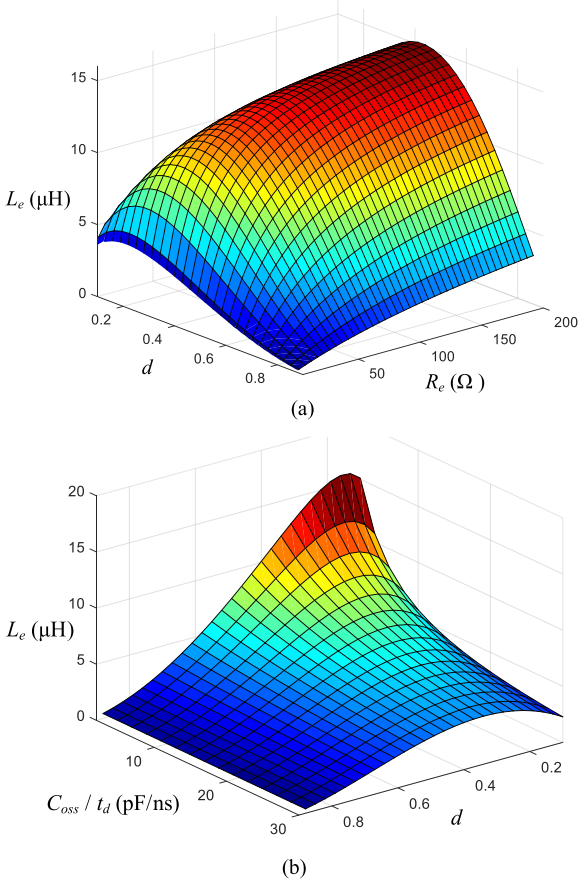


Fig. 11. ZVS turn-ON boundary of switch S_1. (a) Against L_e, R_e, and d. (b) Against L_e, C_{oss} / t_d and d.

Substituting (4), (12), (15), and (18) into (35) gives

$$L_e < \frac{dT}{2(\frac{3C_{oss}}{(1-d)t_d} + \frac{m^2 V_{bus}\sin(\omega t+\varphi)\sin(\omega t)}{|Z_{speaker}|V_{in}(1-d)})}. \tag{36}$$

When the switching period $T = 5$ μs, the dead time $T_{d1} = T_{d2} = 100$ ns, and $C_{oss,s1} = C_{oss,s2} = C_{oss,s3} = 1200$ pF, the ZVS turn-ON boundary of switch S_1 against equivalent inductance L_e, equivalent resistance R_e, and duty ratio d are given as shown in Fig. 11(a).

ZVS turn-ON of switch S_1 can be achieved below the surface shown in Fig. 11(a). It should be noted from Fig. 11(a) that ZVS turn-ON of switch S_1 can be achieved easily with large equivalent resistance R_e, moderate duty ratio d, and small equivalent inductance L_e.

When the switching period $T = 5$ μs, $R_e = 12.5$ Ω, the ZVS turn-ON boundary of switch S_1 against equivalent inductance L_e, the value C_{oss}/t_d and duty ratio d are given as shown in Fig. 11(b).

ZVS turn-ON of switch S_1 can be achieved below the surface shown in Fig. 11(b). It should be noted from Fig. 11(b) that ZVS turn-ON of switch S_1 can be achieved easily with large value C_{oss}/t_d, moderate duty ratio d, and small equivalent inductance L_e.

When (36) is satisfied, ZVS turn-ON of switches $S_1 \sim S_3$ can be achieved over the entire audio output range by design L_e properly. However, if L_e is small, the current i_{L1} or i_{L2} will be high, which will increase copper loss and core loss of the inductors. Therefore, L_e should be designed to meet inequality (36) to achieve ZVS of the switches while being sufficiently large to decrease copper loss and core loss of the inductors.

V. Design of the Controller

State space average method is used to establish a small-signal model of the proposed front-end dc–dc converter, with $\mathbf{x} = [i_{L1}\ i_{L2}\ v_{C1}\ v_{C2}\ v_{C3}]^T$ are state variables and $\mathbf{y} = [y_p\ y_n]^T = [v_{C2}\ v_{C3}]^T$ are output variable. As the dead times are much shorter than the time interval in modes 2 and 4, modes 1 and 3 are neglected. In mode 2, as capacitor C_1 is paralleled with capacitor C_3, the equivalent series resistance R_{C3} of capacitor C_3 is considered to establish state equations.

The state-space average model of the converter is

$$\begin{aligned}\dot{\mathbf{x}} &= ((1-d)\mathbf{A}_1 + d\mathbf{A}_2)\mathbf{x} + ((1-d)\mathbf{B}_1 + d\mathbf{B}_2)v_{in} \\ &= \mathbf{A}\mathbf{x} + \mathbf{B}v_{in} \\ \mathbf{y} &= ((1-d)\mathbf{C}_1 + d\mathbf{C}_2)\mathbf{x} + ((1-d)\mathbf{E}_1 + d\mathbf{E}_2)v_{in} \\ &= \mathbf{C}\mathbf{x} + \mathbf{E}v_{in}\end{aligned} \tag{37}$$

where $\mathbf{x} = \mathbf{X} + \hat{\mathbf{x}}$, $d = D + \hat{d}$ and $v_{in} = V_{in} + \hat{v}_{in}$

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & \frac{d-1}{L_1} & 0 & 0 \\ 0 & 0 & \frac{d}{L_2} & \frac{-1}{L_2} & 0 \\ \frac{1-d}{C_1} & -\frac{d}{C_1} & \frac{R_n+R_{C3}}{R_nR_{C3}C_1}(d-1) & 0 & -\frac{1-d}{R_{C3}C_1} \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{R_pC_2} & 0 \\ 0 & 0 & -\frac{1-d}{R_{C3}C_3} & 0 & \frac{dR_n-R_n-R_{C3}}{R_{C3}C_3(R_n+R_{C3})} \end{bmatrix}$$

$$\mathbf{B} = \begin{bmatrix} \frac{d}{L_1} \\ \frac{d}{L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad \mathbf{C} = \begin{bmatrix} 0\ 0\ 0\ 1 & 0 \\ 0\ 0\ 0\ 0 & \frac{R_n}{R_{C3}+R_n} \end{bmatrix} \quad \mathbf{E} = \mathbf{0}. \tag{38}$$

To simplify the analysis, neglecting the parasitic resistance R_{C3}, then from (37), the steady-state operation point $\mathbf{X}$ is

$$\mathbf{X} = \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \end{bmatrix} = \begin{bmatrix} \frac{D^2R_n+DR_p}{(1-D)^2R_nR_p}V_{in} \\ \frac{D}{(1-D)R_p}V_{in} \\ \frac{D}{1-D}V_{in} \\ \frac{D}{1-D}V_{in} \\ -\frac{D}{1-D}V_{in} \end{bmatrix}. \tag{39}$$

The control-to-output voltage transfer function is

$$G_{y,d}(s) = \begin{bmatrix} G_{v_{po}-d}(s) \\ G_{v_{no}-d}(s) \end{bmatrix} = \begin{bmatrix} \frac{m_1s^2+m_2s+m_3}{(1-D)^2(b_1s^4+b_2s^3+b_3s^2+b_4s+b_5)} \\ \frac{n_1s^3+n_2s^2+n_3s+n_4}{(1-D)^2R_p(b_1s^4+b_2s^3+b_3s^2+b_4s+b_5)} \end{bmatrix} \tag{40}$$

where $G_{vpo\text{-}d}$(s) is the transfer function of control-to-positive output voltage and $G_{vno\text{-}d}$(s) is the transfer function of control-to-negative output voltage.

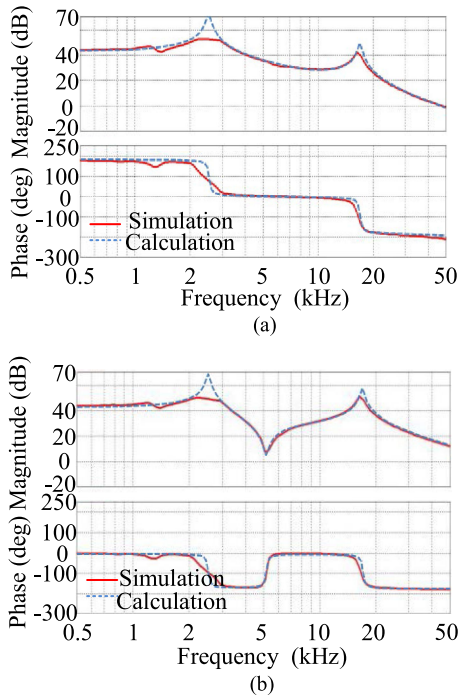


Fig. 12. Bode plots by using MATLAB and PSIM simulation. (a) Control-to-positive output voltage transfer function. (b) Control-to-negative output voltage transfer function.

The audio susceptibility transfer function is

$$G_{y,v_{in}}(s)=\begin{bmatrix}G_{v_{po}-v_{in}}(s)\\ G_{v_{no}-v_{in}}(s)\end{bmatrix}=\begin{bmatrix}\frac{a_1s^2+a_2s+a_3}{(b_1s^4+b_2s^3+b_3s^2+b_4s+b_5)}\\ \frac{c_1s^2+c_2s+c_3}{(b_1s^4+b_2s^3+b_3s^2+b_4s+b_5)}\end{bmatrix} \tag{41}$$

where $G_{vpo\text{-}vin}$(s) is the transfer function of input-to-positive output voltage and $G_{vno\text{-}vin}$(s) is the transfer function of input-to-negative output voltage. The coefficients in (40) and (41) are given below.

Fig. 12(a) and (b) shows the Bode plot of the transfer functions of control-to-positive output voltage and control-to-negative output voltage of the front-end BSO dc–dc converter, respectively. The red solid line denotes PSIM simulation results and the blue dashed line denotes MATLAB calculation results. As shown in Fig. 12, the PSIM simulation results are close to the MATLAB calculation results, which verifies the analysis of the model of the converter.

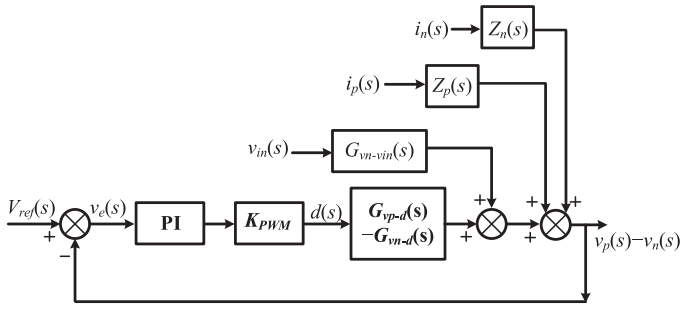


Fig. 13. Control loop of the front-end BSO dc–dc converter.

Fig. 13 shows the control scheme of the front-end BSO dc–dc converter in the proposed HB-CDAA system with conventional voltage control. In the front-end BSO dc–dc converter, the voltage ($v_{C2}-v_{C3}$) is designed as feedback variable, which means the voltage ($v_{C2}+|v_{C3}|$) is controlled. v_{ref}(s) is the reference signal, v_e(s) is the error signal, and d(s) is the duty cycle of switch S_1. PI parameters of the control loop can be designed based on the small-signal model of the converter.

The bode plots are shown in Fig. 12 and the control scheme of the front-end BSO dc–dc converter is shown in Fig. 13. Conventional voltage control and a type II compensator are used in the proposed HB-CDAA system. The 0 dB crossover pole is placed at $f_{p0}=49$ Hz, the pole is placed at $f_{p1}=53$ kHz and the zero is placed at $f_z=1.33$ kHz for the type-II compensator.

Fig. 14 shows the simulation loop gain of the front-end dc–dc converter. It can be observed that phase margin is PM $=45°$ and gain margin is GM $=40$ dB.

VI. Experimental Verification

A. Design Example

To verify the effectiveness of the proposed HB-CDAA system, a 40 W prototype is implemented.

Assume that $T=5\ \mu$s, $t_d=100$ ns, $V_{in}=12$ V, $V_{bus}=24$ V, $Z_{speaker}=4\ \Omega$, $C_{oss,s1}=C_{oss,s2}=C_{oss,s3}=1200$ pF, $m=0.7$

$a_1=DL_1R_nR_p(C_1+C_3)\ a_2=DL_1R_p\ a_3=dR_nR_p(1-D)\ c_1=DC_2R_nR_p(L_1D+L_2D-L_2)\ c_2=DR_n(L_1D+L_2D-L_2)\ c_3=-DR_nR_p(1-D)$

$m_1=V_{in}L_1R_nR_p(C_1+C_3)(1-D)\ m_2=n_2=V_{in}(L_1L_2R_nD+2L_1L_2R_pD+C_2L_1R_nR_p{}^2D+2C_2L_2R_nR_p{}^2D-L_1L_2R_pD^2-C_2L_1R_nR_p{}^2D^2-C_2L_2R_nR_p{}^2D^2-C_2L_2R_nR_p{}^2)V_{in}L_1[R_p-(R_p+R_n)D^2-R_pD]\ m_3=V_{in}R_nR_p(1-D)^2\ n_1=V_{in}C_2L_1L_2R_p(2R_pD+R_nD-R_pD^2)$

$n_2=V_{in}(L_1L_2R_nD+2L_1L_2R_pD+C_2L_1R_nR_p{}^2D+2C_2L_2R_nR_p{}^2D-L_1L_2R_pD^2-C_2L_1R_nR_p{}^2D^2-C_2L_2R_nR_p{}^2D^2-C_2L_2R_nR_p{}^2)$

$n_3=V_{in}(2L_1R_p{}^2D+2L_1R_nR_pD+2L_2R_nR_pD-L_1R_p{}^2D^2-L_1R_nR_pD^2-L_2R_nR_pD^2-L_2R_nR_p)\ n_4=V_{in}R_nR_p(1-D)(R_pD-R_p)$

$b_1=C_1C_2L_1L_2R_nR_p+C_2C_3L_1L_2R_nR_p\ b_2=C_1L_1L_2R_n+C_3L_1L_2R_n+C_2L_1L_2R_p\ b_4=L_1R_nD^2+L_2R_nD^2-2L_2R_nD+L_2R_n+L_1R_p$

$b_3=C_1L_1R_nR_p+C_2L_2R_nR_p+C_3L_1R_nR_p+C_2L_1R_nR_pD^2+C_2L_2R_nR_pD^2-2C_2L_2R_nR_pD+L_1L_2\ b_5=R_nR_p-2R_nR_pD+R_nR_pD^2$

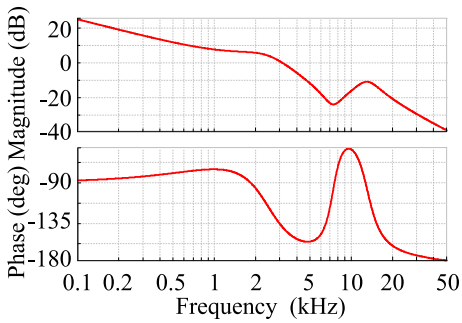


Fig. 14. Loop gain of the front-end BSO dc–dc converter.

TABLE I
DESIGN SPECIFICATIONS AND CIRCUIT PARAMETERS

Input / Output Voltage, V_{in} / V_{out}	10~14V / ±24V
Output Power, P_{out}	40W
Switching Frequency, f_s	200kHz
Dead time, t_d	100ns
Inductor L_1 / L_2	4.2μH / 4.2μH
Capacitor C_{in}, C_1, C_2 and C_3	47μF
Switches S_1, S_2 and S_3	BSC016N06NS
Half bridge class-D audio amplifier	IRAUDAMP-7
Speaker load resistor	4Ω

and $\varphi = \pi/6$, from (36), L_e should satisfy $L_e < 2.12\ \mu$H. In this article, $L_e = 2.1\ \mu$H is designed, and inductances $L_1 = L_2 = 4.2\ \mu$H are adopted. Since the inductors L_1 and L_2 are operated with the same steady-state voltages, they also can be combined into single coupled inductor to reduce the number of magnetics components and improve the power density.

The voltage ripples across capacitors C_1-C_3 are related to the capacitances C_1-C_3. In the proposed HB-CDAA system, the voltage ripples across capacitors C_1-C_3 are [33]

$$\Delta v_{C1} = \frac{dTI_o}{2C_1} \tag{42}$$

$$\Delta v_{C2} = \frac{\Delta i_{L2} T}{8C_2} \tag{43}$$

$$\Delta v_{C3} = \frac{\Delta i_{L1} T}{8C_3}. \tag{44}$$

Usually, output voltage ripple should be less than 2% of the output voltage. From (28)–(29) and (42)–(44), if $V_{in} = 12$ V, $V_{C2} = 24$ V, $T = 5\ \mu$s, $L_1 = L_2 = 4.2\ \mu$H, and $I_o = 1$ A, to ensure output voltage ripple is 2% of the output voltage, it should have $C_1 = C_2 = C_3 = 6.6\ \mu$F. When the equivalent series resistance (ESR) of the capacitors is considered, the capacitance of capacitors $C_1 - C_3$ should be larger than the calculated value. Therefore, $C_1 = C_2 = C_3 = 47\ \mu$F is selected in the prototype to ensure output voltage ripple is less than 2% of output voltage.

Fig. 15 shows the prototype of the front-end BSO dc–dc converter in the proposed HB-CDAA system, and Table I gives the design specifications and circuit parameters.

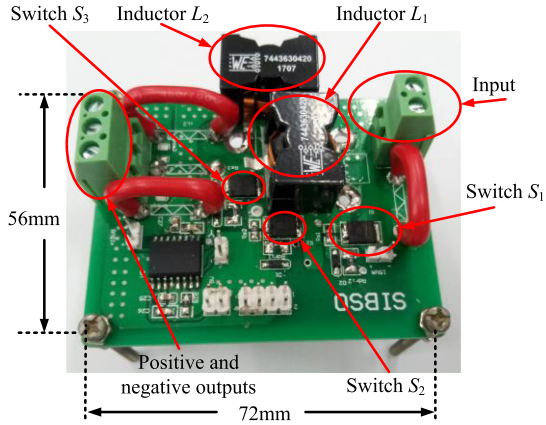


Fig. 15. Prototype of the front-end BSO dc–dc converter in the proposed HB-CDAA system.

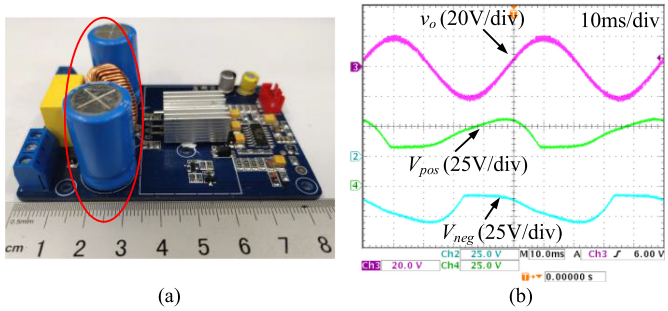


Fig. 16. Conventional HB-CDAA system. (a) HB-CDAA with large electrolytic. (b) Bus voltage with bus-voltage capacitors pumping.

VII. EXPERIMENTAL RESULTS

As the average power of audio amplifier is 1/8–1/3 full power when the audio amplifier operates with music or voice, the heatsink on the downstream HB-CDAA is designed according to the loss at 1/3 full power [34]. The maximum loss of downstream HB-CDAA is around 2.4 W when the efficiency of downstream HB-CDAA is 82% in the conventional and the proposed HB-CDAA systems. Thus, the heatsink with dimensions W: 2 cm, L: 2 cm, H: 0.9 cm is used in the conventional and the proposed HB-CDAA system.

Fig. 16(a) shows the prototype of downstream HB-CDAA in the conventional HB-CDAA system, where 470 μF(63 V) electrolytic capacitors are used as positive and negative bus capacitances $C_{\rm pos}$ and $C_{\rm neg}$ to reduce the bus-voltage pumping. Fig. 16(b) shows that severe bus-voltage pumping across capacitors $C_{\rm pos}$ and $C_{\rm neg}$ remains even though large bus capacitors are adopted.

Fig. 17(a) shows the prototype of downstream HB-CDAA in the proposed HB-CDAA system, where positive and negative bus capacitors C_2 and C_3 both are 47 μF(35 V). As shown in Fig. 17(b), bus-voltage pumping is eliminated in the proposed HB-CDAA system, and large electrolytic capacitors are not required.

Compared with a conventional unidirectional bipolar front-end dc–dc converter in [12]–[14] as shown in Fig. 4(a), the

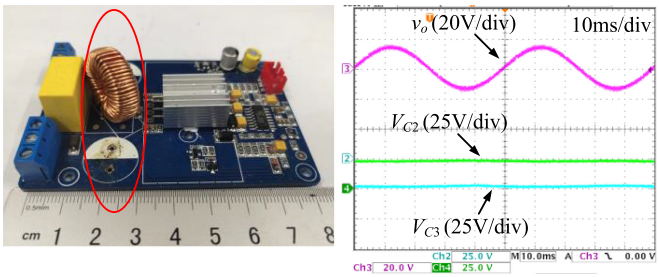


Fig. 17. Proposed HB-CDAA system. (a) HB-CDAA without electrolytic. (b) Bus voltage without bus-voltage capacitors pumping.

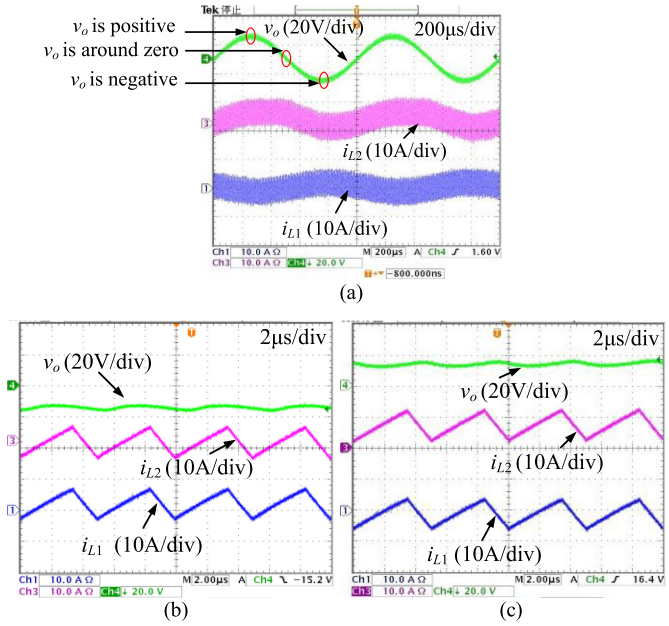


Fig. 18 . Key waveforms of the proposed HB-CDAA system. (a) Currents i_{L1} and i_{L2}. (b) Currents i_{L1} and i_{L2} when $v_o < 0$. (c) Currents i_{L1} and i_{L2} when $v_o > 0$.

proposed HB-CDAA system needs one more MOSFET, but without two diodes in the front-end dc–dc converter. Furthermore, in the proposed HB-CDAA system, the large electrolytic capacitors C_{pos} and C_{neg} are removed, and soft switching of front-end dc–dc converter is achieved. Figs. 16(a) and 17(a) show that the power density of downstream HB-CDAA is improved by removing the large electrolytic capacitors.

As shown in Fig. 18(a), the load voltage v_o of HB-CDAA system can be positive, zero, and negative. Since a 4 Ω resistor load is used in the prototype, the load current i_o is in phase with load voltage v_o. Fig. 18(b)–(c) shows current waveforms of i_{L1} and i_{L2} when load voltage v_o is negative and positive, which are in consistent with the analysis in Fig. 8.

Fig. 19(a)–(i) shows drain-source voltage $v_{\rm DS}$ and drain-source current i_{ds} of the MOSFETs $S1$–$S3$ in the front-end BSO dc–dc converter of the proposed HB-CDAA system. It can be observed that ZVS turn-ON of switches $S1$–$S3$ can be realized at different load current conditions.

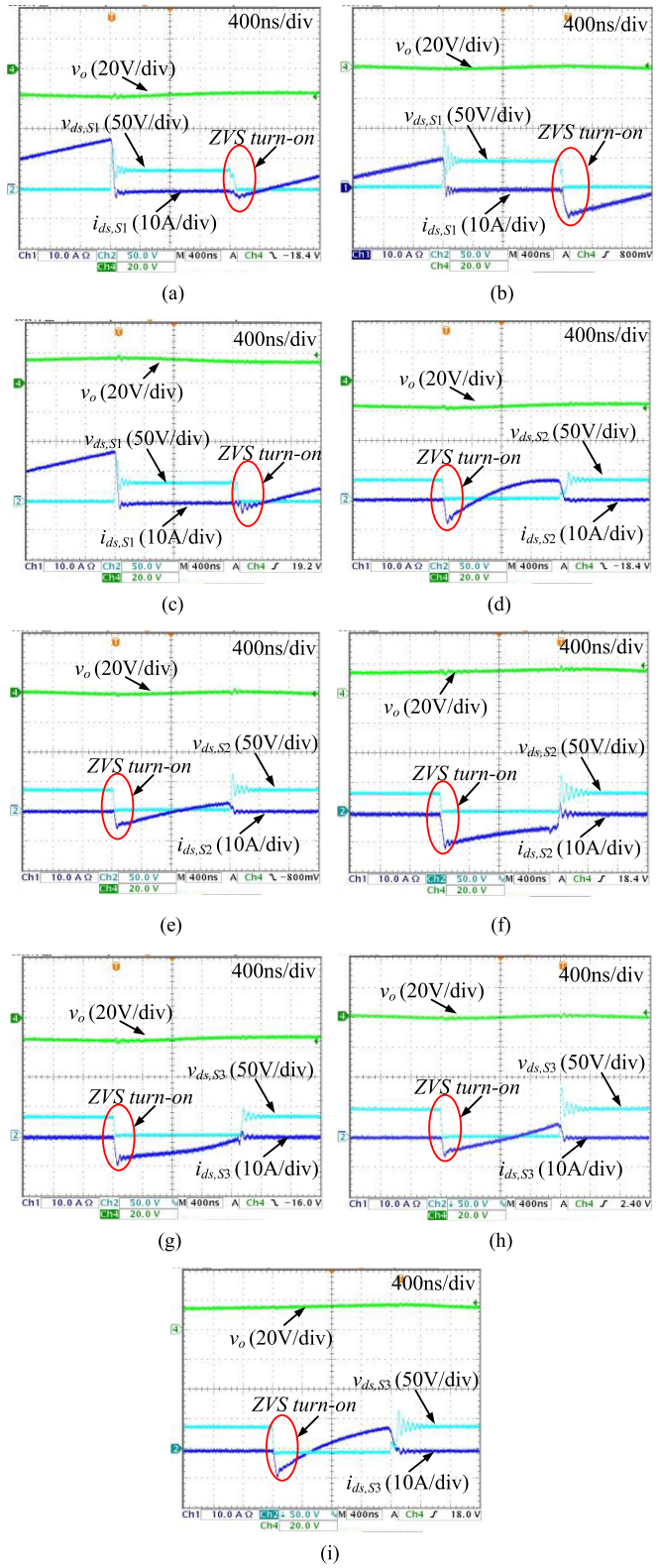


Fig. 19. Waveforms of ZVS turn-ON of switches. (a) ZVS turn-ON of switch S_1 when $i_o < 0$. (b) ZVS turn-ON of switch S_1 when $i_o = 0$. (c) ZVS turn-ON of switch S_1 when $i_o > 0$. (d) ZVS turn-ON of switch S_2 when $i_o < 0$. (e) ZVS turn-ON of switch S_2 when $i_o = 0$. (f) ZVS turn-ON of switch S_2 when $i_o > 0$. (g) ZVS turn-ON of switch S_3 when $i_o < 0$. (h) ZVS turn-ON of switch S_3 when $i_o = 0$. (i) ZVS turn-ON of switch S_3 when $i_o > 0$.

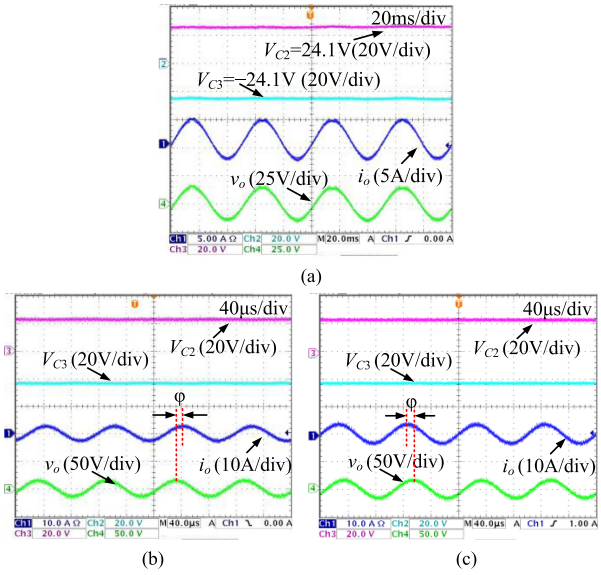


Fig. 20. Key waveforms of the proposed HB-CDAA system under different loads. (a) Resistive load. (b) Inductive load. (c) Capacitive load.

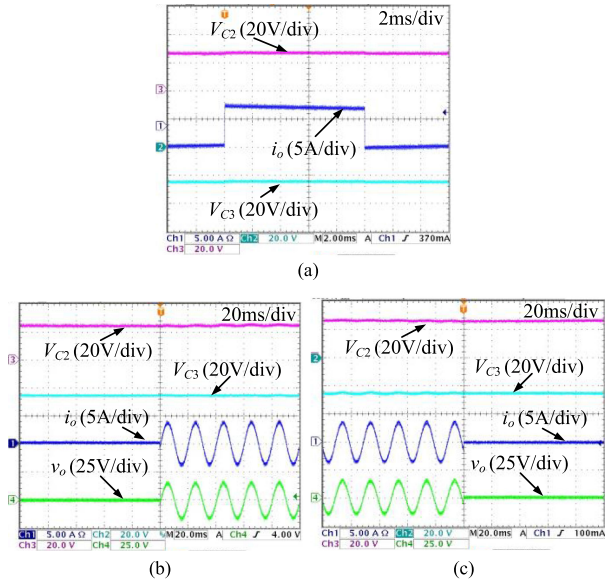


Fig. 21. Dynamic performance of the proposed HB-CDAA system. (a) Step load between 4 and -4 A for square output frequency. (b) Step load increase from 0 to 3 A. (c) Step load decrease from 3 to 0 A for 50-Hz sinusoidal output frequency for 50-Hz sinusoidal output frequency.

Fig. 20(a)–(c) shows waveforms of bus voltages, load voltage v_o, and load current i_o under resistive, inductive, and capacitive load, respectively. Fig. 20(a) shows a 20-Hz sinusoidal load voltage v_o with 4 Ω resistor load, the load current i_o is in phase with load voltage v_o. Fig. 20(b) shows a 10-kHz sinusoidal load voltage v_o with an inductive load of 4 Ω resistor in series with 40 μH inductor, and the load current i_o lags load voltage v_o. Fig. 20(c) shows a 10-kHz sinusoidal load voltage v_o with a capacitive load of 4 Ω resistor in series with 6.6 μF capacitor, and the load current i_o leads load voltage v_o. These waveforms show the proposed HB-CDAA system can operate at the four-quadrants under different loads with bus-voltage pumping eliminated.

Fig. 21(a)–(c) shows the dynamic performance of the proposed HB-CDAA system with a 4 Ω resistor load. Fig. 21(a) shows that the load current varies between 4 and -4 A. Fig. 21(b) shows a step load increase from 0 to 3 A (rms value) with a 50-Hz sinusoidal output, and Fig. 21(c) shows a step load decrease from 3 (rms value) to 0 A with a 50-Hz sinusoidal output. Fig. 21 shows that the bus voltage for downstream HB-CDAA V_{C2} and V_{C3} are stable when load current steps. Thus, the proposed HB-CDAA system has good dynamic performance.

As nonlinearity in the PWM signal, dead time, finite switching speed, parasitic parameters, ripple of power supply, nonlinearity in the output filter, etc., would cause the output voltage distortion in CDAA [35], [36]. To verify the output voltage distortion caused by the bus-voltage pumping, the same downstream HB-CDAAs are used in the conventional and the proposed HB-CDAA system to compare the output voltage THD+N with or without bus-voltage pumping.

Fig. 22 shows the THD measurement procedure of the proposed HB-CDAA system. In the proposed HB-CDAA system, the front-end BSO dc–dc converter is connected with the downstream HB-CDAA, the audio reference signal is given by the

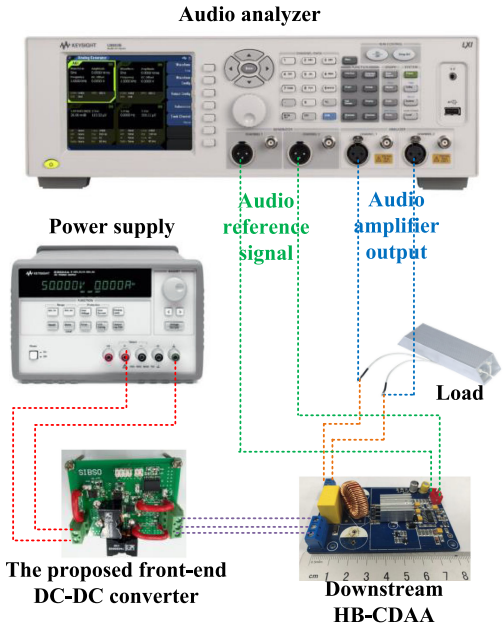


Fig. 22. THD measurement procedure of the proposed HB-CDAA system.

U8903B audio analyzer, and the output of the HB-CDAA system is connected to the audio analyzer to measure the output voltage THD+N. For comparison, the output voltage THD+N of the conventional HB-CDAA system is also measured.

Fig. 23(a) and (b) shows the comparison of output voltage THD+N against different audio output frequencies or different audio output powers between the proposed HB-CDAA system and the conventional HB-CDAA system, similar to Fig. 4(a). Bus-voltage pumping is not present in the proposed HB-CDAA, unlike in the conventional HB-CDAA even with large bus capacitors are used. Therefore, the output voltage THD+N would

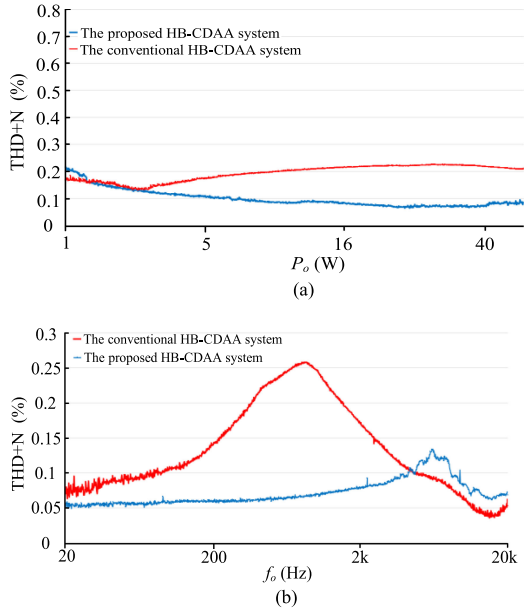


Fig. 23. Comparison of output voltage THD+N between the proposed HB-CDAA system and conventional HB-CDAA system. (a) Output voltage THD+N against different audio output power. (b) Output voltage THD+N against different audio output frequency.

be worse in the conventional HB-CDAA when the downstream HB-CDAAs are the same in the two systems.

As shown in Fig. 23(a), when the frequency of the audio signal is 1 kHz and the output power is low, the output voltage THD+N is similar in the two systems since the modulation index m in (2) and (3) is very small and bus-voltage pumping is not severe. When the output power is high, the bus-voltage pumping is high in the conventional HB-CDAA system, thus the output voltage THD+N in the conventional HB-CDAA system is worse than that in the proposed HB-CDAA system.

Generally, the HB-CDAA has high PSRR for low-frequency bus-voltage pumping and low PSRR for high-frequency bus-voltage pumping [1]. As shown in Fig. 23(b), when the frequency of the audio signal is lower than 100 Hz at half load, although the bus-voltage pumping is severe in the conventional HB-CDAA system, the THD+N is similar in the two systems due to high PSRR of downstream HB-CDAA. When the frequency of the audio signal is 100 Hz–2 kHz, as the bus-voltage pumping is still severe and PSRR is not very high in the conventional HB-CDAA system, the THD+N of conventional HB-CDAA system is around 0.2% higher than that in the proposed HB-CDAA system. When the frequency of the audio signal is higher than 5 kHz, bus-voltage pumping is very small according to (2) and (3), thus the THD+N is similar between conventional HB-CDAA system and the proposed HB-CDAA system.

From Fig. 23, the experimental results verify the theoretical analysis. The elimination of bus-voltage pumping allows the proposed HB-CDAA system to have a lower output voltage THD+N than that in the conventional HB-CDAA system.

Table II gives the loss calculation of the proposed front-end BSO dc–dc converter.

TABLE II
LOSS ANALYSIS OF THE FRONT-END BSO DC–DC CONVERTER

P_{S1}	$P_{con,S1}$	$I_{S1,rms}{}^2 R_{ds(on)}$ ($I_{S1,rms}$ is RMS value of drain-to-source current through switch S_1, $R_{ds(on)}$ is on-state resistance of the MOSFET)	1066mW
	$P_{off,S1}$	$\frac{1}{2}t_f(V_{in}-V_{C3})(i_{L1,\max}+i_{L2,\max})f_s$ $=\frac{1}{2}t_f(\frac{V_{in}}{1-d})(\frac{dV_{in}R_n+dV_{in}R_p}{(1-d)^2R_pR_n}+\frac{V_{in}}{2L_1}dT+\frac{V_{in}}{2L_2}dT)f_s$ (t_f is falling time of the MOSFET)	
	P_{driver}	$v_g Q_g f_s$	
P_{S2}	$P_{con,S2}$	$I_{S2,rms}{}^2 R_{ds(on)}$ ($I_{S2,rms}$ is RMS value of drain-to-source current through switch S_2, $R_{ds(on)}$ is on-state resistance of the MOSFET)	187mW
	$P_{off,S2}$	$\frac{1}{2}t_f(V_{in}-V_{C3})(-i_{L1,\min})f_s$ $=\frac{1}{2}t_f(\frac{V_{in}}{1-d})(\frac{V_{in}}{2L_1}dT-\frac{d^2V_{in}R_n+dV_{in}R_p}{(1-d)^2R_pR_n})f_s$ (t_f is falling time of the MOSFET)	
	P_{driver}	$v_g Q_g f_s$	
P_{S3}	$P_{con,S3}$	$I_{S3,rms}{}^2 R_{ds(on)}$ ($I_{S3,rms}$ is RMS value of drain-to-source current through switch S_3, $R_{ds(on)}$ is on-state resistance of the MOSFET)	459mW
	$P_{off,S3}$	$\frac{1}{2}t_f(V_{in}+V_{C1})(-i_{L2,\min})f_s$ $=\frac{1}{2}t_f(\frac{V_{in}}{1-d})(\frac{V_{in}}{2L_2}dT-\frac{dV_{in}}{(1-d)R_p})f_s$ (t_f is falling time of the MOSFET)	
	P_{driver}	$v_g Q_g f_s$	
P_{L1}	P_{cupper}	$I_{L1}{}^2 R_{ac,L1}$ ($R_{dc,L1}$, $R_{ac,L1}$, $I_{dc,L1}$, and $I_{ac,L1}$ are the DC resistance, the AC resistance, the average current, and the AC RMS current of the winding of inductor L_1, respectively)	907mW
	P_{core}	$P_v V$ (P_v is constants, which are related to material and ΔB, V is the volume of the core of inductor L_1, ΔB satisfies $\Delta B=\frac{V_{L1}t}{nS}=\frac{V_{in}dT}{2nS}$, n is turns of inductor L_1, S is cross sectional area of the core of inductor L_1)	
P_{L2}	P_{cupper}	$I_{L2}{}^2 R_{ac,L2}$ ($R_{dc,L2}$, $R_{ac,L2}$, $I_{dc,L2}$, and $I_{ac,L2}$ are the DC resistance, the AC resistance, the average current, and the AC RMS current of the winding of inductor L_2, respectively)	453mW
	P_{core}	$P_v V$ (P_v is constants, which are related to material and ΔB, V is the volume of the core of inductor L_2, ΔB satisfies $\Delta B=\frac{L_2 i_{L2,peak}}{nS}=\frac{L_1}{nS}[\frac{dV_{in}}{(1-d)R_p}+\frac{V_{in}}{2L_2}dT]$, n is turns of inductor L_2, S is cross sectional area of the core of inductor L_2)	
P_C	$P_{C1}+P_{C2}+P_{C3}$	$I_{C1,rms}{}^2 R_{ESR,C1}+I_{C2,rms}{}^2 R_{ESR,C2}+I_{C3,rms}{}^2 R_{ESR,C3}$ ($R_{ESR,C1}$, $R_{ESR,C2}$ and $R_{ESR,C3}$ are equivalent series resistance of capacitors C_1, C_2 and C_3. $I_{C1,\text{rms}}$, $I_{C2,\text{rms}}$ and $I_{C3,\text{rms}}$ are RMS value of the current through capacitors C_1, C_2 and C_3.)	153mW

According to Table II, the loss breakdown of the front-end BSO dc–dc converter at full load is given in Fig. 24. Fig. 25 shows the thermal images of the front-end BSO dc–dc converter at 30 and 40 W load with no thermal compound, heatsink, or fan cooling. As shown in Fig. 25(a) and (b), the temperature of switch S_1 and inductors L_1 and L_2 is high, and the highest

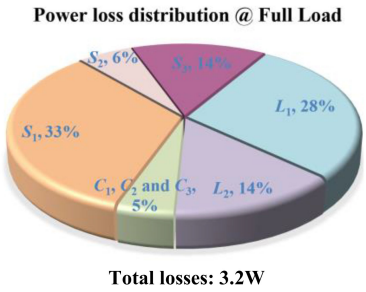


Fig. 24. Loss breakdown of the front-end BSO dc–dc converter at full load.

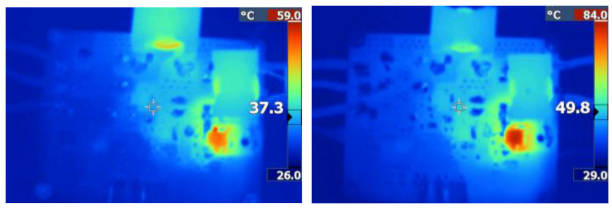


Fig. 25. Thermal performance of the front-end BSO dc–dc converter (no thermal compound, heatsink or fan cooling). (a) 30 W load. (b) 40 W load.

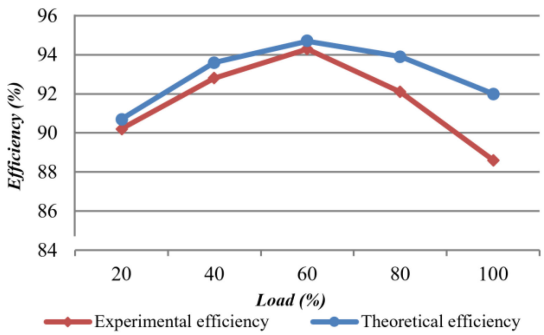


Fig. 26. Experimental efficiency of the proposed front-end BSO dc–dc converter.

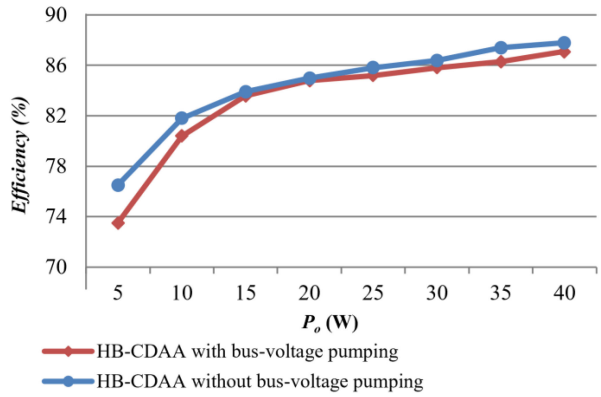


Fig. 27. Experimental efficiency of downstream HB-CDAA with or without bus-voltage pumping.

TABLE III
COMPARISON BETWEEN THE PROPOSED FRONT-END BSO DC–DC CONVERTER AND THE REFERENCES

References		[16]		[25]		[26]		This work	
Switch		2		2		4		3	
Diode		4		4		2		0	
Inductor		1		0		0		2	
Transformer		1		1		1		0	
Input	Output	10~16V	±18V	311V	±50V	311V	±54V	10V~14V	±24V
Switching frequency		100kHz		100kHz		200kHz		200kHz	
Capability of output voltage regulation		Yes		No		No		Yes	
Input capacitances		Small		Large		Large		Small	
Bus capacitances		940μF(35V)		1410μF (100V)		20μF(63V)		47μF(35V)	
Voltage stress across the bus capacitor		High		High		Low		Low	
Bus-voltage pumping		Severe		Severe		No		No	
Output power		60W		100W		200W		40W	
Peak efficiency		88.3%		96.5%		96.3%		94.3%	

temperature spot is on the switch S_1, which is in consistent with the theoretical analysis in Table II.

From the analysis in Table II and the measured results, Fig. 26 gives the theoretical and experimental efficiency of the front-end BSO dc–dc converter in the proposed HB-CDAA system with 40-W rated output power. Because ZVS turn-ON is achieved in the front-end BSO dc–dc converter of the proposed HB-CDAA system, the peak efficiency of the front-end BSO dc–dc converter is 94.3% at 60% rated load.

As shown in Fig. 27, the efficiency curves of the downstream HB-CDAAs in the conventional and the proposed HB-CDAA system are given, respectively. Since the conventional HB-CDAA system has severe bus-voltage pumping and the proposed HB-CDAA system eliminates the bus-voltage pumping, the voltage stress of the downstream HB-CDAA in a conventional HB-CDAA system is higher than that in the proposed HB-CDAA system. Thus, the switching loss of downstream HB-CDAA is higher, and the efficiency of downstream HB-CDAA is consequently lower in the conventional HB-CDAA system.

Table III shows the comparison between the proposed front-end BSO dc–dc converter and the recent other front-end converters for HB-CDAA. A front-end dc–dc converter is presented in [16], and two front-end DCXs are proposed in [25] and [26] for the HB-CDAA system. As the converter in [16] and [25] can only provide a unidirectional current path for the downstream HB-CDAA, severe bus-voltage pumping occurs and thus large electrolytic capacitors are required to reduce the pumping. Although the DCX in [26] can provide a bidirectional current path, large electrolytic capacitors are still required at the input terminal to provide a stable power supply for the downstream HB-CDAA as the DCXs in [25] and [26] have no capability of output voltage regulation. The proposed front-end BSO dc–dc converter eliminates the bus-voltage pumping without electrolytic bus capacitor in the entire HB-CDAA system, achieves high efficiency, and high power density.

VIII. Conclusion

In this article, a novel HB-CDAA system is proposed. In the proposed HB-CDAA system, both step-up or step-down voltage gain and stable symmetric bipolar outputs are obtained in the front-end BSO dc–dc converter, which provides a high-quality power supply for the downstream HB-CDAA. By providing a bidirectional current flowing path for the downstream HB-CDAA, bus-voltage pumping of the proposed HB-CDAA system is eliminated without large electrolytic capacitors, which improves output voltage THD+N, reduces voltage stress of the HB-CDAA, and achieves ZVS of switches of the front-end converter over the entire load current range. Compared with the conventional HB-CDAA system with a unidirectional front-end dc–dc converter, the proposed audio amplifier system benefits from a power density improvement of downstream HB-CDAA, a 94.3% peak efficiency of the front-end dc–dc converter, a lower output voltage THD+N, and voltage stress of switches in the HB-CDAA. The proposed HB-CDAA system is thus suitable for some multichannels audio amplifier applications which need high efficiency, high power density, and low THD+N.

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